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100 APPLICATION LAYER 102 -104 s s S OPERATING SYSTEM 106 KERNEL 112 DISPATCHER 114 -120 s S S RUN QUEUES 124a-n 111b -108a-n 126b 111n 111a~ -126n 126a-~110n PHYSICAL PROCESSING 110b MODULES 110a-n 110a

Fig. 1A

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Date of Deposit: September 12, 2003

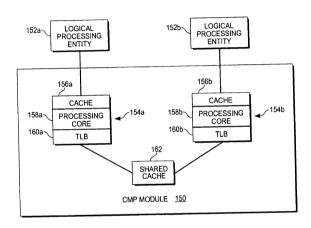


Fig. 1B

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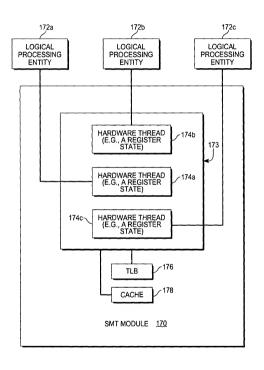


Fig. 1C

Date of Deposit: September 12, 2003

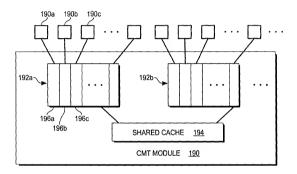


Fig. 1D

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200 APPLICATION LAYER 202 -204 S S S S OPERATING SYSTEM 206 216 214 KERNEL 212 ABSTRACTION DISPATCHER MANAGER ABSTRACTIONS 222a-n 220 ABSTRACTION LAYER 222 s S S -220 224a-n RUN QUEUES 208a-n

Fig. 2A

- 211a-n

~210n

210a-n

PHYSICAL PROCESSING

MODULES

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210c

SMT

210b

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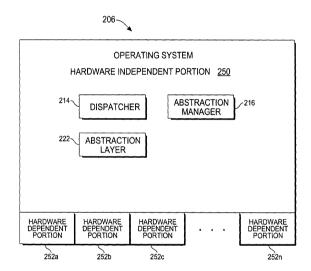


Fig. 2B

Inventor(s): Eric C. Saxe, et al.

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Date of Deposit: September 12, 2003 15437-0579 7 of 12 210c SHARED CACHE THREADED CMT MODULE C326b LOGICAL PROCESSING ENTITY 318 314a HARDWARE THREAD (E.G., A REGISTER STATE) HARDWARE THREAD (E.G., A REGISTER STATE) 210b HARDWARE THREAD (E.G., A REGISTER STATE) LOGICAL PROCESSING ENTITY -312b 314b SMT MODULE -314c CACHE 138 LOGICAL PROCESSING ENTITY 312a LOGICAL PROCESSING ENTITY PROCESSING CORE CACHE 1LB 306b 210a SHARED SMP MODULE 302b -302a 304b/ 308a

PROCESSING ENTITY

306a

304a

PROCESSING CORE CACHE

밀 306 310a

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ABSTRACTION 400

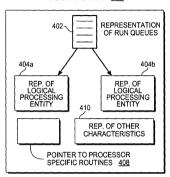
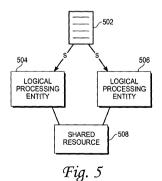


Fig. 4



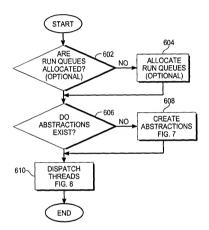
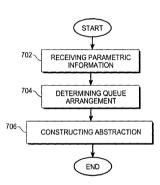


Fig. 6

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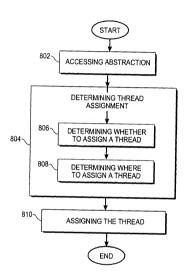


Fig. 8

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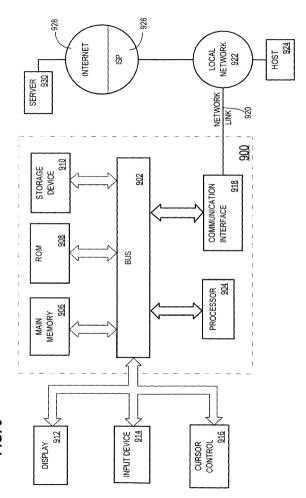


FIG. 9